REMARKS/ARGUMENTS

Favorable reconsideration of this application is respectfully requested.

An objection was made to the drawings as not showing the feature "each of the second switching elements has a plurality of transistor elements" recited in claim 5. This language is deleted from claim 5, and thus withdrawal of the objection to the drawings is respectfully requested.

Claims 1, 2, 4-8, and 10-21 are present in this application. Claims 1, 2, 4-8 and 10-21 are rejected under 35 U.S.C. §112, first paragraph. Claims 16 and 17 are rejected under 35 U.S.C. §112, second paragraph. Under 35 U.S.C. §103(a), claims 5-7, 10, 15, 20 and 21 are rejected over U.S. 6,765,549 (Yamazaki et al.) in view of U.S. 7,133,013 (Kamezaki et al.), and claims 1, 2, 4 and 16-19 are rejected over Yamazaki et al. in view of U.S. 6,583,775 (Sekiya et al.) and Kamezaki et al.

Claims 1, 2 and 5 are amended to recite "moves the plurality of stripe non-display areas in a scanning direction of the gate driver circuit at cycle of one frame period." This language finds support in the non-limiting disclosure of Figs. 16, 17 and 19(c). Gate driver circuit 12 moves the plurality of stripe non-display areas 52a-52d on display screen 50 in a scanning direction of the gate driver circuit 12 at a cycle of one frame period. The image is later displayed. No question of introduction of new matter is believed to be raised.

With regard to the §112, second paragraph, rejection, claims 16 and 17 are amended to recite "transistors," to correct a typographical error. Withdrawal of the rejection of claims 16 and 17 under §112, second paragraph, is respectfully requested.

The §112, first paragraph, rejection is based upon not finding support for "an image signal applied to each pixel is executed only once during the one frame." This feature is shown, for example, in the non-limiting disclosure of Figure 17(a) where gate signal line applies an ON signal (Vg1) to transistor 11c during the period (1H) for selecting one pixel

row only once during the one frame period (1F), and then the image signal is written into each pixel 16. Accordingly, this disclosure clearly supports the subject matter of claims 1 and 2 regarding the image signal applied to the pixel being executed only once during the one frame period. Withdrawal of the §112, first paragraph, rejection of claims 1 and 2 is respectfully requested.

Secondly, the Office Action did not find support for the language in claim 5 "each of the second switching elements has a plurality of transistor elements." This language has been deleted from claim 5, and the §112 rejection of claim 5 is now moot.

Lastly, the "p-channel resistors" recited in claims 16 and 17 was also found to lack support in the specification. These claims are amended to correct a typographical error, as discussed above, and withdrawal of the §112, first paragraph, rejection of claims 16 and 17 is respectfully requested.

Claims 1 and 2 recites a drive method for an EL display panel, and claim 5 recites an EL display panel. In the panel of the method of claim 1, and the panel of claim 5, first switching elements are placed in current paths of the EL elements. A non-limiting example of the switching elements is provided by switch 11d where, as shown in Fig. 3, switch 11d is placed between EL element 15 and driver transistor 11a, that is, in the current path.

The Office Action relies upon Yamazaki et al. for this feature, referring to TFT 105 and EL element 111. On the contrary, TFT 105 applies an image signal (a source signal) to an SRAM 108 and Vout of the SRAM 108 is connected to the gate electrode of EL driver TFT 109 as driver transistor. A current path of the EL element is through the source and drain of driver TFT 109, and not through its gate. Therefore, it is clear that TFT 105 is not placed in current path of the EL element. The first switching elements placed in current paths of the EL elements are not disclosed by Yamazaki et al. The remaining two cited references,

Kamezaki et al. and Sekiya et al. also do not disclose this feature, nor are they asserted to disclose this feature.

Claim 1 also recites that the gate driver circuit generates a plurality of stripe non-display areas on a display screen of the EL display panel by controlling the first switching elements in an off-state two or more times during one frame period. Claim 5 recites that the first gate driver circuit generates a plurality of stripe non-display areas on display screen of the EL display panel by controlling the first switching elements in an off-state during one frame period. The first switching element is placed in a current path of the EL element. The current path of the EL element is thus in an on-off-state two or more times during one frame period. By controlling the first switching elements in such manner, a plurality of stripe non-display areas on display screen of the EL display panel are generated.

The Office Action on page 8 refers controlling TFT 105 in an off-state two or more times during one frame period by driver 103. However, TFT applies an image signal to SRAM 108 two or more times during one frame period. A plurality of stripe non-display areas are not generated by controlling TFTs 105. The cited prior art also does not disclose these features of claims 1 and 5.

Claims 1, 2 and 5 each recite that the plurality of stripe non-display areas are moved in the scanning direction of the gate driver circuit at a cycle of one frame period. In Figure 3 of Yamazaki et al., TFT 105 is controlled in an on-off-state two or more times during one frame period. On the contrary, the "first switching element" of the present invention is placed in a current path of the EL element (for example, placed between the EL element 15 and the driver transistor 11a) and is switched in the current path of the EL element in an off-state two or more times during one frame period. In the present invention, by controlling the first switching elements in such manner, a plurality of stripe non-display areas on display screen of the EL display panel are generated.

Therefore, even if TFT 105 in Figure 3 of Yamazaki et al. is controlled in an on-off-state two or more times during one frame period, Yamazaki et al. cannot "generate a plurality of stripe non-display areas on display screen of the EL display panel."

Claims 1, 2 and 5 recite that an operation for retaining an image signal applied to each pixel is executed only once during the one frame period. In the non-limiting example described above, switching transistor 11c applies the image signal to driver transistor 11a and the operation for retaining an image signal applied to each pixel is executed only once (1H, as shown in Figure 17(a)) during one frame period (1F, as shown Figure 17(a)). In Yamazaki et al., TFT 105 applies image signal to the SRAM 108 two or more times during one frame period. The Office Action looks to Sekiya et al. which describes continuing to display an image for one frame. However, there is no explanation how such operation would be applied to Yamazaki et al., and there is no explanation of how this relates to the TFT 105 which supplies the image signal twice during one frame period, or how one frame period. The combination of Yamazaki et al. with Sekiya et al. does not suggest this feature of claims 1, 2 and 5.

Claims 1, 2 and 5 also recite that the plurality of stripe non-display areas are moved in a scanning direction of the gate driver circuit at a cycle of one frame period. This feature can reduce the power consumption, reduce the generation of the flicker and control the display brightness of the screen. The Applicants have prepared the attached pages to help better understand this feature, prepared with relation to the non-limiting disclosure in the present specification. In the first page ("Display Control"), the movement of the non-display areas in the scanning direction is illustrated. The second page illustrates on-off operation of transistors 11d, while the third page illustrates possible display control (brightness) with movement of the non-display areas at a cycle of one frame period.

The Office Action refers to Kamezaki et al. for this feature of the claims. Kamezaki et al. discloses a liquid crystal display device which generates non-display portion in a part of the display screen. However, the liquid crystal display device has the non-display portions 1b and 1c and the display portion la which are partitioned in the direction of the scanning signal lines (see column 7, lines 8-20). Therefore, it is clearly that these non-display portions are fixed in the display screen and not moved in scanning direction of the gate driver circuit at cycle of one frame period. Kamezaki et al. is clearly quite different from the methods of claims 1 and 2 and the panel of claim 5.

Numerous features of claims 1, 2 and 5 are not found in or suggested by the cited prior art. Therefore, claims 1, 2 and 5 are patentably distinguishable over Yamazaki et al. considered alone or with Kamezaki et al. and/or Sekiya et al.

Since claims 4, 6, 7, 10 and 15-21 depend from claims 1, 2 and 5, these dependent claims are patentable over the applied prior art for the same reasons respectively discussed above for claims 1, 2 and 5.

It is respectfully submitted that the present application is in condition for allowance, and a favorable action to that effect is respectfully requested.

Respectfully submitted,

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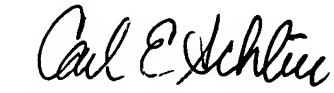

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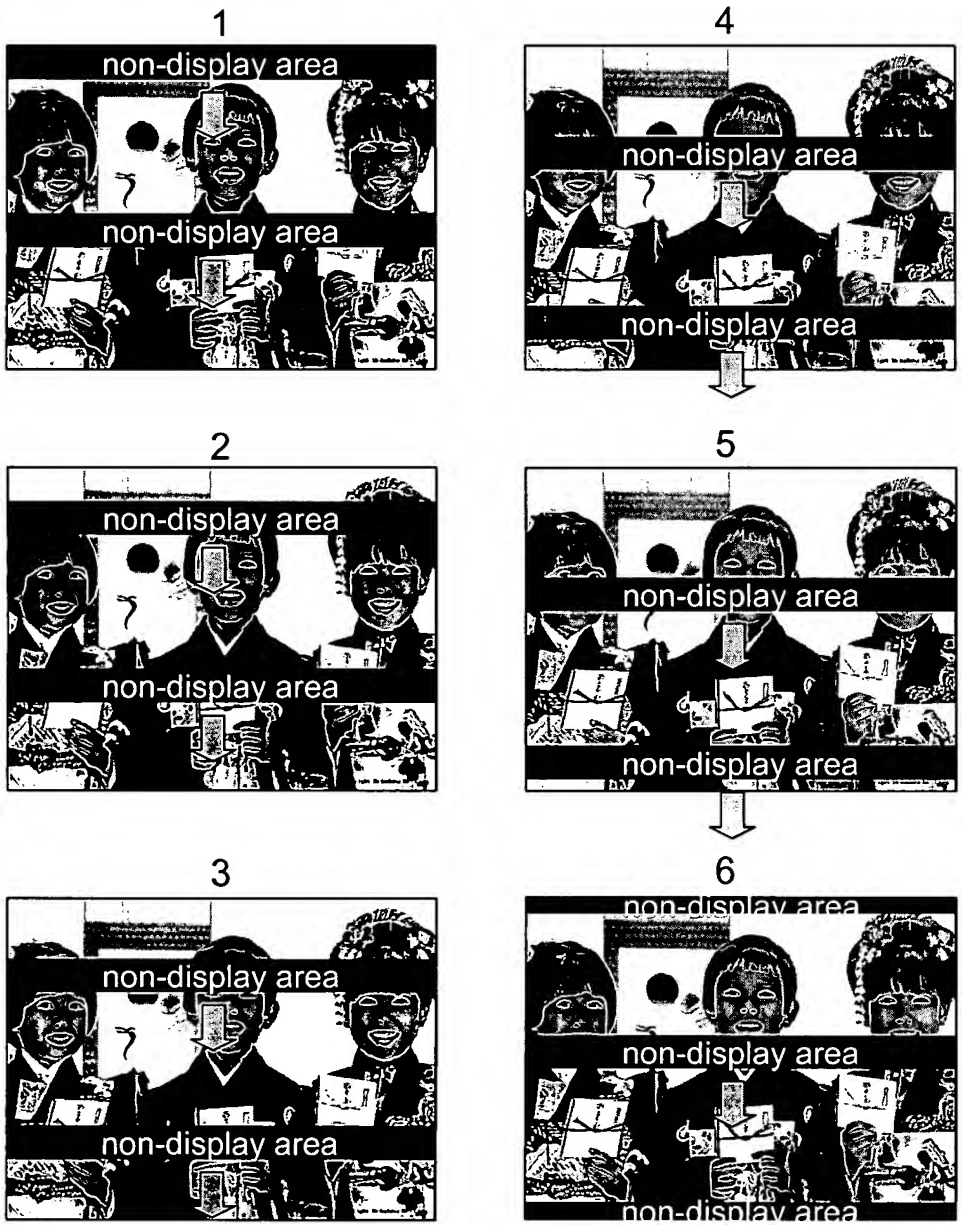
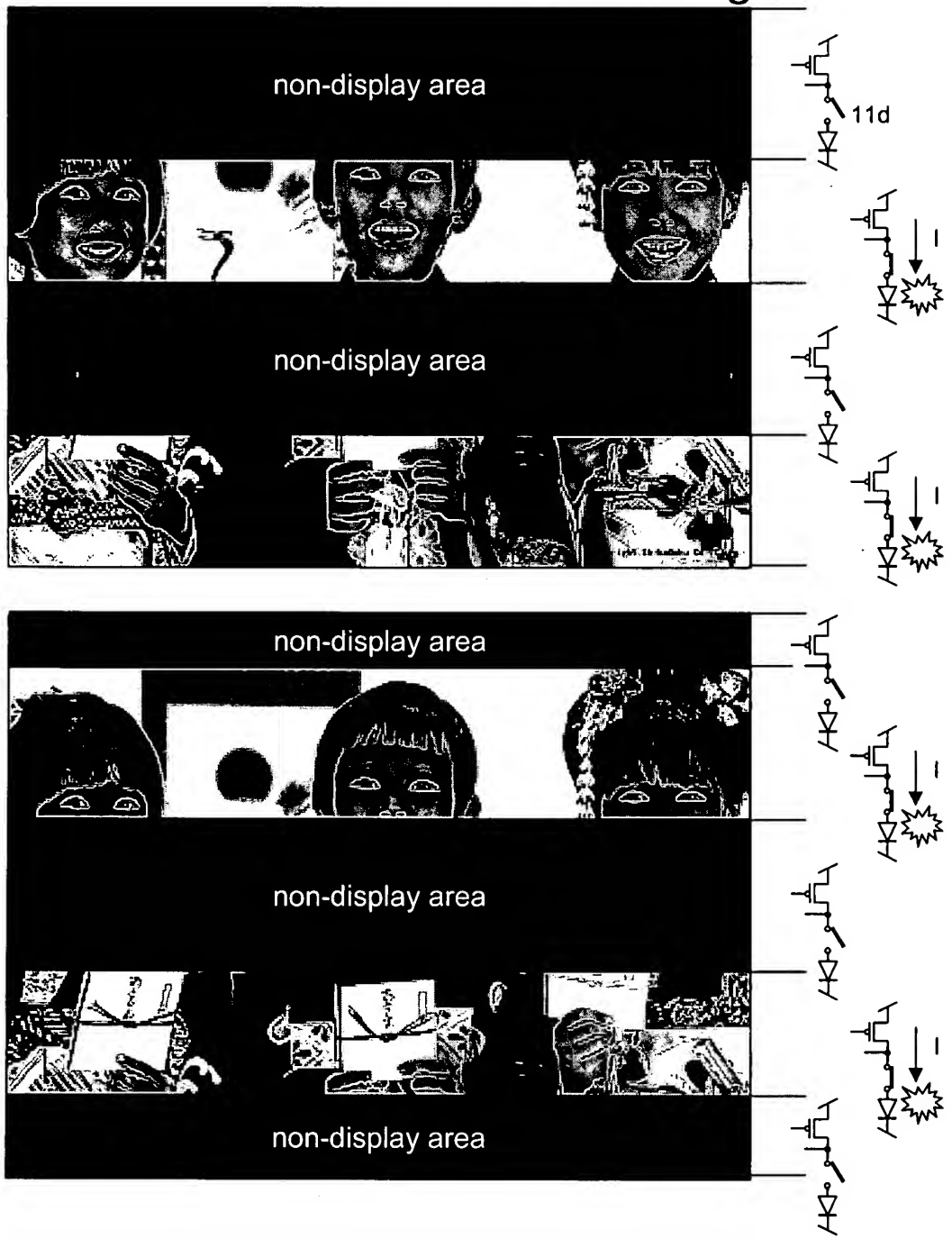
Display control



1 frame

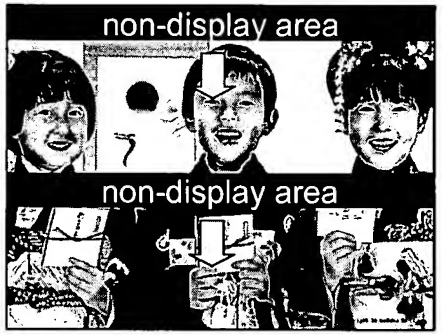
1→2→3→4→5→6

The movement of the switching transistor11d

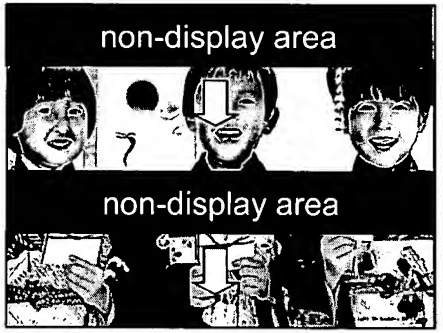


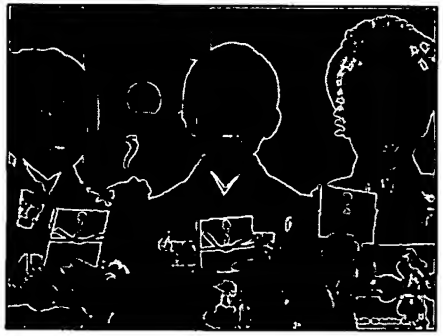
Display image

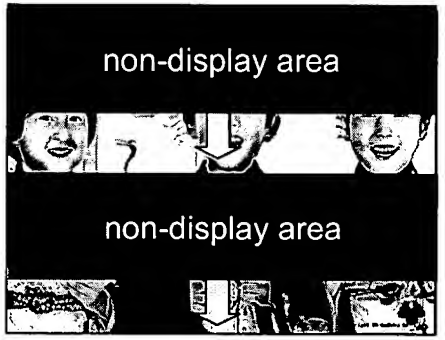
Display control



Brightness is high







Brightness is low

RELATED CASE STATUS UPDATE

Instant Application No: 10/511,447

Jun-01-2009

Application No / Control No	PTO Action Description	PTO Mail Date	Applicant Action Description	Date Filed
10/511,437	Final Rejection	Dec-31-2008		
10/511,448	Office Action	Mar-26-2009		
10/555,642	Notice of Allowance	Apr-15-2009		
10/555,460	Final Rejection	Jan-05-2009		